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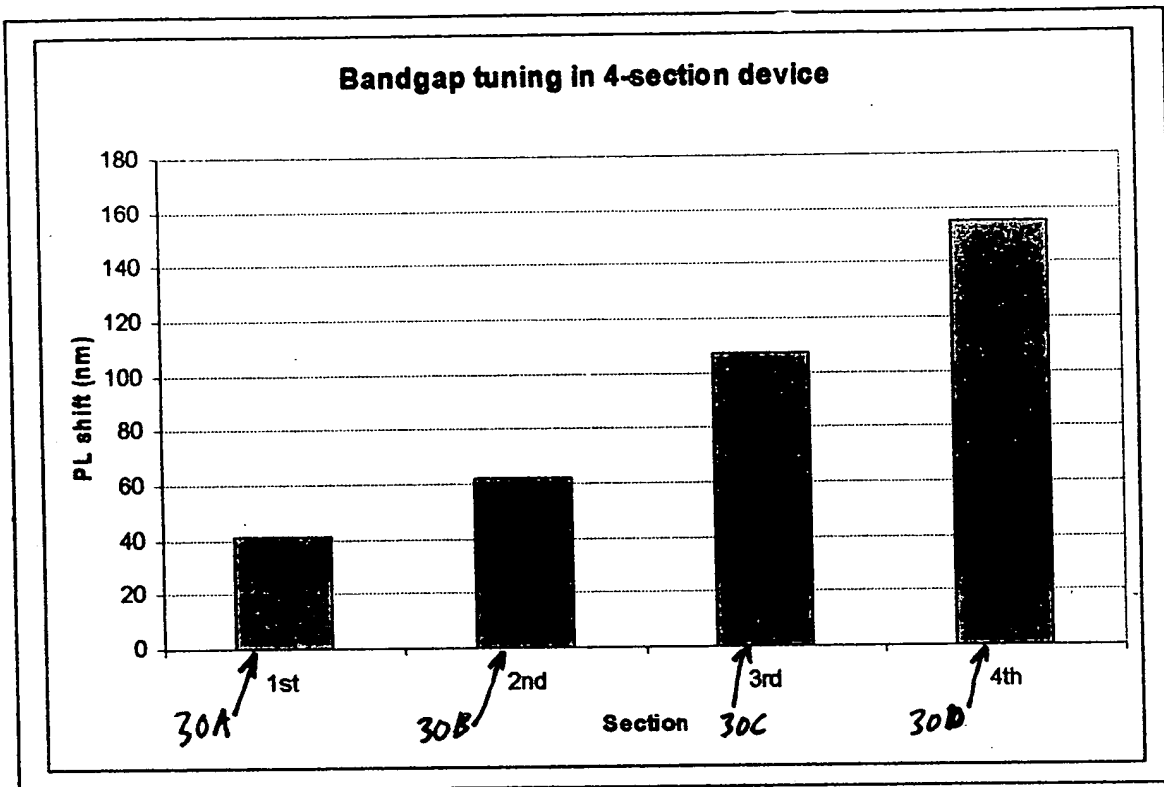


Figure 2

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FIG. 3A

(a) patterning of the as-grown wafer

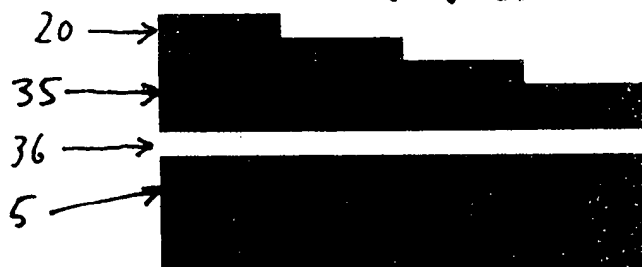


FIG. 3B

(b) patterning of the as-grown wafer, dielectric cap deposition and RTA



FIG. 3C

(c) remove all sacrificial layers for further processing of the device wafer

Device wafer

sacrificial layer

Etch stop

Dielectric cap

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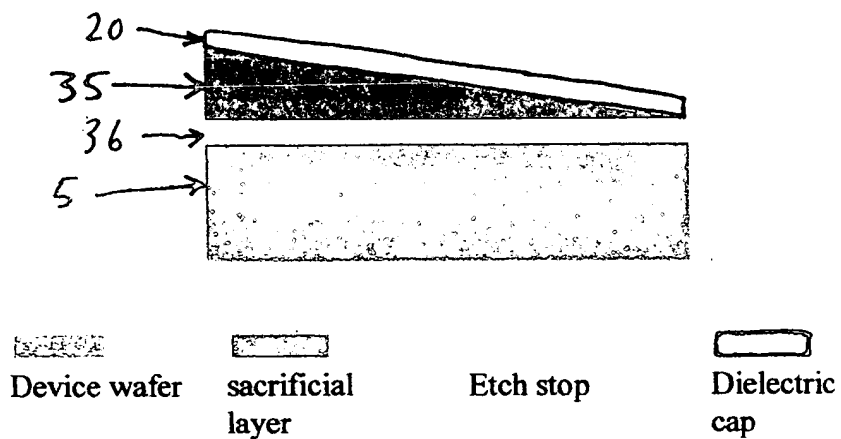


Figure 4

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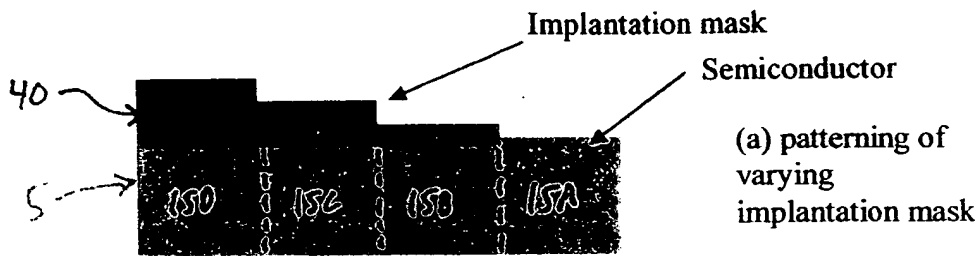


FIG. 5A

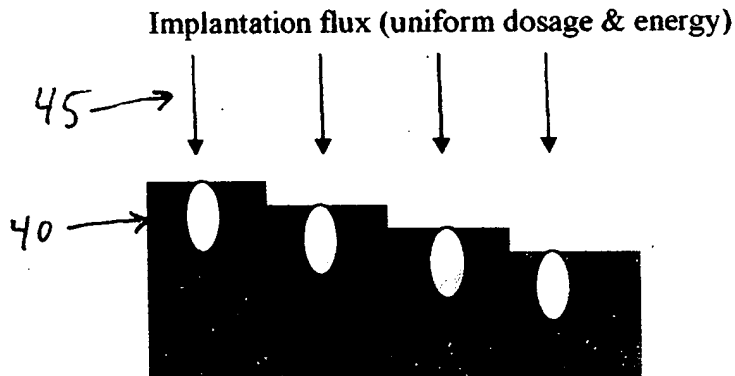


FIG. 5B

Left-over implantation damage in semiconductor

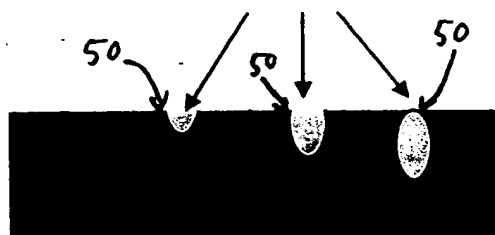


FIG. 5C

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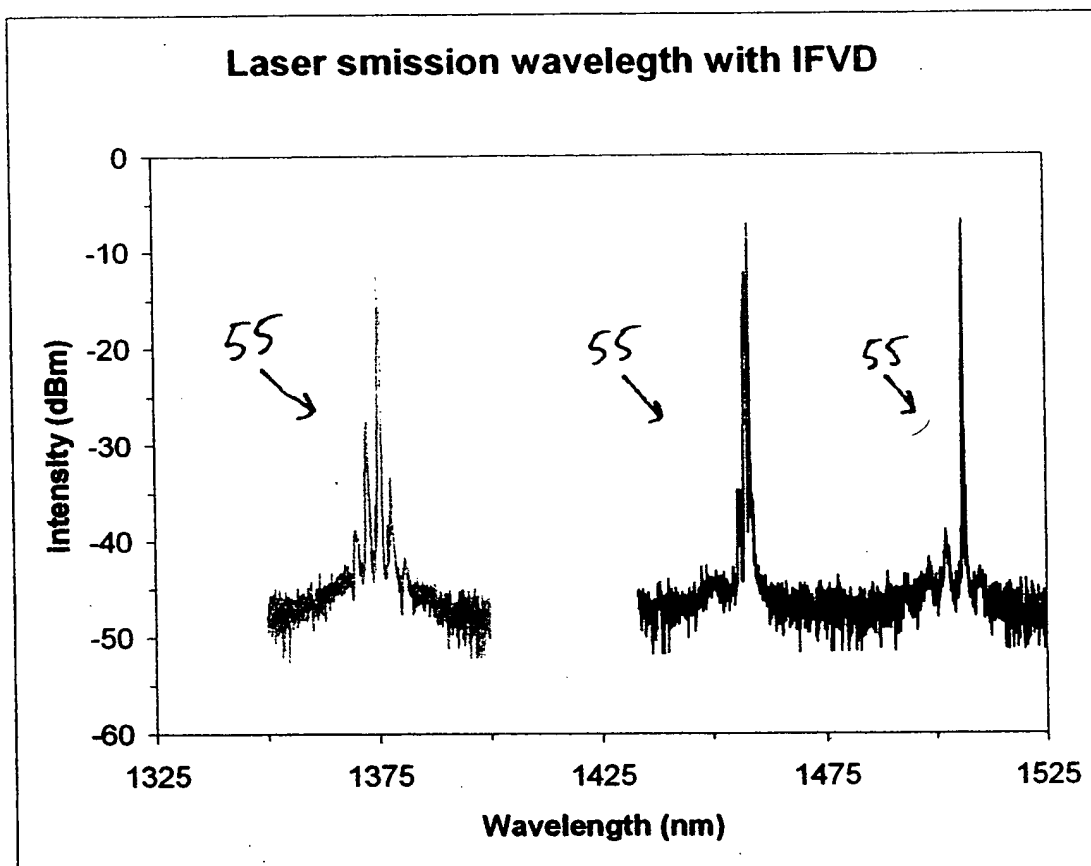


FIG. 6

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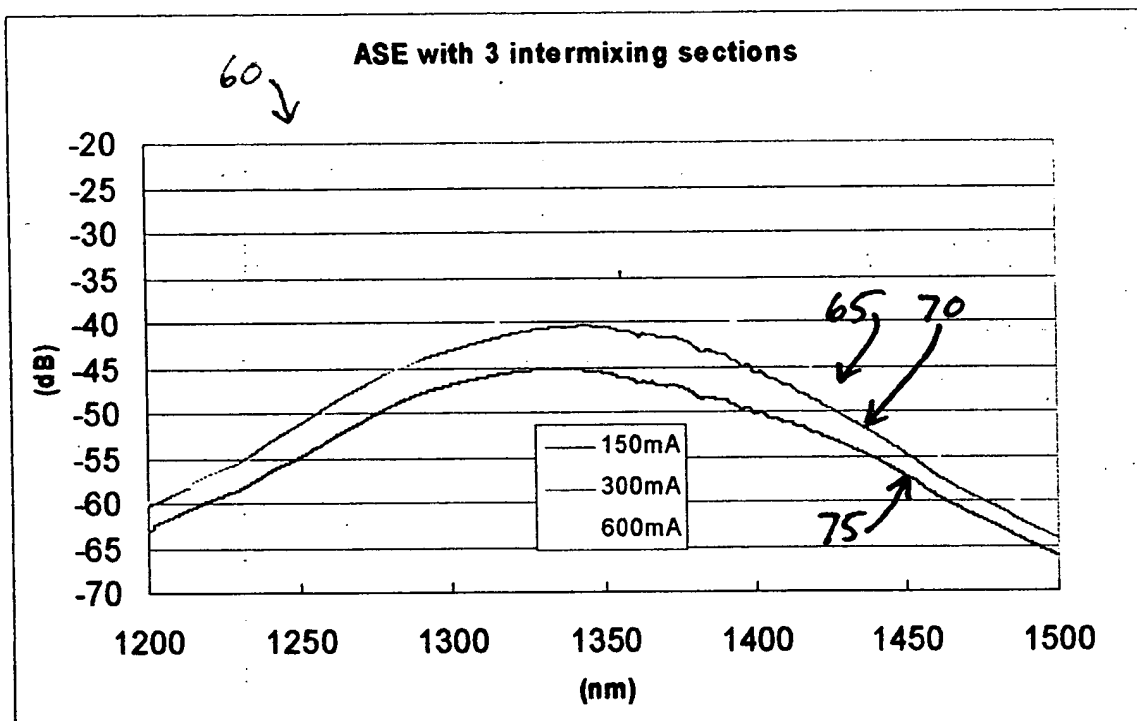


FIG. 7

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